Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-18 (Canceled)

Claim 19 (New): A semiconductor device comprising:

a semiconductor substrate;

a source region and a drain region formed in the semiconductor substrate;

a first insulating layer formed on the semiconductor substrate;

a gate electrode structure formed on the first insulating layer, the gate electrode structure having a lower gate electrode layer and a cap gate layer formed on the lower gate electrode layer;

a side wall structure which includes a nitride side wall spacer, and includes a CVD oxide layer formed between the semiconductor substrate and the nitride side wall spacer and between the lower gate electrode layer and the nitride side wall spacer;

a second insulating layer covering the gate electrode and the side wall structure, the second insulating layer having a first contact hole exposing the source region and a second contact hole exposing the drain region; and

a conductive material embedded in the first and second contact holes,

wherein a thickness of the CVD oxide layer is greater than a thickness of the first insulating layer so as to prevent diffusion of nitrogen from the side wall spacer to the semiconductor substrate, and

wherein a thickness of the gate electrode structure including the cap gate layer is substantially equal to a height of the side wall structure after completion of the semiconductor device.

Claim 20 (New): The semiconductor device of claim 19, wherein the side wall structure is exposed in the first or second contact holes.

Claim 21 (New): The semiconductor device of claim 19, wherein the thickness of the CVD oxide layer between the semiconductor substrate and the nitride side wall spacer is at least twice the thickness of the first insulating layer.

Claim 22 (New): The semiconductor device of claim 19, wherein the thickness of the CVD oxide layer between the semiconductor substrate and the nitride side wall spacer is at least 50% greater than the thickness of the first insulating layer.

Claim 23 (New): The semiconductor device of claim 19, wherein the CVD oxide layer prevents diffusion of nitrogen from the side wall structure into the source and the drain regions.

Claim 24 (New): The semiconductor device of claim 19, wherein the CVD oxide layer is formed on side surfaces of the cap gate layer.

Claim 25 (New): The semiconductor device of claim 19, wherein the CVD oxide layer is not formed on side surfaces of the cap gate layer.

Claim 26 (New): The semiconductor device of claim 19, wherein the first insulating layer is silicon oxide.

Claim 27 (New): A semiconductor device comprising:

a semiconductor substrate;

a source region and a drain region formed in the semiconductor substrate;

a first insulating layer formed on the semiconductor substrate, the first insulating layer having a pair of first portions located on the source region and the drain region, and having a second portion located between the first portions;

a gate electrode structure formed on the second portion of the first insulating layer, the gate electrode structure having a lower gate electrode layer and a cap gate layer formed on the lower gate electrode layer;

a supplemental oxide insulating layer formed on the gate electrode structure;

a side wall structure which includes a nitride side wall spacer, and includes a

CVD oxide layer formed between the semiconductor substrate and the nitride side wall spacer;

a second insulating layer covering the gate electrode structure and the side wall structure, the second insulating layer having a first contact hole exposing the source region and a second contact hole exposing the drain region; and

a conductive material embedded in the first and second contact holes so as to contact the source region and the drain region,

wherein a thickness of the CVD oxide layer is greater than a thickness of the second portion of the first insulating layer so as to prevent diffusion of nitrogen from the nitride side wall spacer to the semiconductor substrate, and

wherein a thickness of the gate electrode structure including the cap gate layer is substantially equal to a height of the side wall structure after completion of the semiconductor device.

Claim 28 (New): The semiconductor device of claim 27, wherein the side wall structure is exposed in the first or second contact holes.

Claim 29 (New): The semiconductor device of claim 27, wherein a combined thickness of the first portion of the first insulating layer and the CVD oxide layer between the semiconductor substrate and the nitride side wall spacer is at least twice a thickness of the second portion of the first insulating layer.

Claim 30 (New): The semiconductor device of claim 27, wherein a combined thickness of the first portion of the first insulating layer and the CVD oxide layer between the semiconductor substrate and the nitride side wall spacer is at least 50% greater than a thickness of the second portion of the first insulating layer.

Claim 31 (New): The semiconductor device of claim 27, wherein the CVD oxide layer prevents diffusion of nitrogen from the side wall structure into the source region and the drain region.

Claim 32 (New): The semiconductor device of claim 27, wherein the CVD oxide layer is formed on side surfaces of the cap gate layer.

Claim 33 (currently amended): The semiconductor device of claim 27, wherein the CVD oxide layer is not formed on side surfaces of the cap gate layer.

Claim 34 (New) The semiconductor device of claim 27, wherein the first insulating layer and the CVD oxide layer are silicon oxide.